WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a control block comprising:

a first series of delay elements coupled to a reference clock input, each delay element having an input;

a first selection circuit coupled to a plurality of inputs of the first series of delay elements;

a phase detector coupled to the reference clock input and an output of the selection circuit; and

a counter coupled to the phase detector and the series of delay elements; and

a delay circuit coupled to the counter.

2. The integrated circuit of claim 1 wherein the first selection circuit comprises a multiplexer.

3. The integrated circuit of claim 1 wherein the delay circuit comprises:

a second series of delay elements, each having an input; and

a second selection circuit coupled to a plurality of inputs of the second series of delay elements.

4. The integrated circuit of claim 3 wherein an output of the second selection circuit couples to a first storage element.

5. The integrated circuit of claim 4 wherein the first storage element is a flip-flop.

6. The integrated circuit of claim 4 wherein an output of the second selection circuit couples to a clock input of a first flip-flop and a complementary clock input of a second flip-flop.

7. The integrated circuit of claim 6 wherein the first and second flip-flops are coupled to a data input.

8. The integrated circuit of claim 3 wherein the integrated circuit is a field programmable gate array.

9. An integrated circuit comprising:

a control circuit configured to receive a reference clock and provide a plurality of control bits; and

a delay line configured to receive the plurality of stored control bits wherein the delay line comprises:

a first series of delay elements each having an input; and

a first select circuit configured to a plurality of inputs of the first series of delay elements.

10. The integrated circuit of claim 10 wherein the first select circuit is a multiplexer.

11. The integrated circuit of claim 10 wherein the control circuit comprises:

a second series of delay elements configured to receive the reference clock, each delay element having an input; and

a second select circuit coupled to a plurality of inputs of the second series of delay elements.

12. The integrated circuit of claim 11 wherein the control circuit further comprises:

a phase detector configured to compare the phases of the reference clock and an output of second select circuit and provide an output signal; and

a counter configured to receive the phase detector output and provide the control bits.

13. The integrated circuit of claim 12 wherein a polarity of the phase detector output depends on the relative phase of the reference clock and the output of second select circuit, and the counter is an up-down counter that counts up when the phase detector output has a first polarity, and counts down when the phase detector output has a second polarity.

14. The integrated circuit of claim 11 wherein the first series of delay elements is configured to delay a read strobe signal.

15. The integrated circuit of claim 15 further comprising a storage element configured to receive an output of the first select circuit.

16. The integrated circuit of claim 10 wherein the control circuit is a delay-locked loop.

17. The integrated circuit of claim 10 wherein the integrated circuit is a field programmable gate array.

18. A method of delaying a data strobe signal comprising:

receiving a reference clock signal;

delaying the reference clock signal using a first number of delay elements, each delay element providing a delayed reference clock signal;

selecting one of the delayed reference clock signals;

comparing the phase the reference clock signal and the selected delayed reference clock signal to generate the plurality of control signals; and

delaying the data strobe signal using a second number of delay elements.

19. The method of claim 18 wherein each of the second number of delay elements provide a delayed strobe signal; and the method further comprises:

selecting one of the delayed strobe signals.

20. The method of claim 19 further comprising:

receiving a data signal using the selected one of the delayed strobe signals.